SILICON-ON-INSULATOR DEVICE

TECHNICAL FIELD

This invention relates to Silicon On Insulator (SOI) devices, and more particularly, to an SOI device suitable for use in a bias condition wherein the substrate layer, sometimes called the "wafer handler" layer, is maintained at a potential in between that of the source and drain regions.

BACKGROUND OF THE INVENTION

Figure 1 shows a cross section of a typical prior art high voltage Silicon On Insulator (SOI) device. The device 100 in Figure 1 includes the typical components and regions thereof, such as the source 101, drain 103 and gate region 102. The buried oxide layer 104 forms a junction with the SOI layer 105, both disposed above the substrate layer 106. Such devices are, in many applications, utilized in a bias condition wherein the source 101, substrate 106, and gate 102 are maintained at ground potential, while the drain region 103 is maintained at or near 200 volts. Such bias conditions are typical in a variety of switching applications relating to medical and communications technology, as well as other technological fields.

Such a device can easily support the 200 volts applied to the drain in an off state with a drift length of approximately 12 micrometers.

Although the configuration of Figure 1 works well when the device is biased as described, various applications require a different type of biasing. More specifically, in certain switching operations it is necessary to apply a relatively large positive voltage to the drain, and a relatively large negative voltage to the source and gate, while maintaining the substrate voltage at approximately ground. In such configurations, it is typical to bias the source and gate at approximately negative 100 volts, the drain at approximately positive 100 volts, and the substrate layer at approximately 0 volts. This bias condition is referred to as source below substrate potential. Such a condition is employed in a wide variety of circuitry with telephony, medical, and other applications. In such a condition, the substrate is maintained at a voltage between that of the source and drain, rather than the substrate being maintained at a voltage substantially the same as that of the source, as was described with respect to the prior art.

Figure 3 shows the simulation of the device of Figure 1 biased in a source below substrate bias condition. Although an attempt is made to bias the source at negative 100

volts and the drain at plus 100 volts, the device can only maintain a maximum difference of approximately 65 volts between the source and drain. The problem is that the breakdown voltage of the device falls from over two hundred volts when it is biased as described with respect to the prior art, to approximately 65 volts when the biasing condition is changed to source below substrate. Accordingly, there exists a need in the art for a thin layer SOI switching device that can operate in the source below bias condition without suffering breakdown at a relatively low voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 depicts a prior art silicon on insulator thin layer switching device;

Figure 2 depicts the electric fields generated within the device of Figure 1 at particular bias conditions;

Figure 3 depicts an exemplary embodiment of the invention;

Figure 4 shows an electric field diagram simulating operation of the device of Figure 3 in a particular bias condition.

SUMMARY AND DETAILED DESCRIPTION OF THE INVENTION

In accordance with the invention, the P inversion region in the device is extended to include a "tongue", or extension, which extends into the junction between the buried oxide layer and the silicon on insulator layer. The additional P-type doping that forms the extension or tongue is chosen such that it is depleted by the bias applied to the substrate layer. The depletion of this additional P-type doping means that any bias applied to the drain will deplete n-type charge in the N-Well region 316, shown in Figure 3. This affect lowers the electric field in the vicinity of the junction between the N-Well region 316 and the P-inversion region 318. By lowering this electric field, the drain voltage can be increased to very near the 200 volts that the device would sustain when biased as described above with respect to the prior art.

Figure 3 shows an exemplary embodiment of the present invention including a substrate layer 304, a buried oxide layer 312, an SOI layer 310, source, gate and drain regions 309, 302, and 314, respectively. The N-Well region of the device includes negative charge as indicated at 316 in Figure 3. Additionally, the P-inversion region 318 is shown having a short extension or a "tongue" 303, which extends into the junction between the buried oxide layer 312 and the SOI layer 310. Although the extension 303 is shown as a tongue shape and is referred to by that term, the invention is not limited to shaping the extension in such a manner, and those of skill in the art will recognize that the additional p-

type atoms introduced within extension may be introduced as other shapes, so long as the charge volumes and concentrations are sufficient. Typical charge levels in the tongue region (integrated vertically through the p-type extension) range from 5e11 to 1 e12 cm-2.

In operation according to source below bias condition, the source 309 is biased at, for example, negative 100 volts while the drain 314 would be biased to positive 100 volts. The substrate layer 304 is maintained at approximately ground, leaving 100 volts between the substrate and either the source or drain.

The problem of relatively low breakdown voltages is eliminated by the addition of P-type charge in the small extension or tongue 303. More specifically, the additional charge within the extension region 303 is largely depleted by the bias applied to substrate 304. The positive bias then applied to the drain acts to deplete n-type charge in region 316, just adjacent to the P-inversion/N-Well layer junction, labeled 330. This phenomenon results in a much lower lateral electric field across the junction 330 adjoining P-inversion region 318 with N-Well region 316. The lower electric field means that the drain can be maintained at a higher voltage, thus eliminating the relatively low breakdown voltage for source below substrate bias conditions.

It has been determined empirically that the extension of tongue may be ideally fabricated by using a 1.5 MeV implant of Boron with a fluence of 3e12 cm-2. A photo resist mask is used to properly apply the shape and endpoints of the extension structure, which typically extend 2-3um past the edge of the PI diffusion region into the drift region. This technique can be integrated with standard diffused channel (LDMOS) process flows or with Latid (large angle tilt implant technology) for PI region formation.

While the above describes the preferred embodiment of the invention, various modifications or additions would be apparent to those of skill in the art. For example, the tongue or extension need not be shaped exactly as shown, but need only provide the sufficient charge so that the bias applied to the substrate layer serves first to deplete that charge, leaving the N-Well charge to be depleted by the drain voltage. Boron need not be used, but any suitable P-type charge can be used to lower the effective lateral electric field in the vicinity of the P-inversion/N-Well junction 330 . Rather than the biases given, other biases, such as, for example, 50 volts at the drain and negative 50 at the source, can be used.